74AHC573; 74AHCT573

Octal D-type transparant latch; 3-state

Rev. 03 — 24 April 2008 Product data sheet

1. General description

The 74AHC573; 74AHCT573 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7A.

The 74AHC573; 74AHCT573 consists of eight D-type transparent latches featuring separate D-type inputs for each latch and 3-state true outputs for bus oriented applications. A latch enable input (LE) and an output enable input ($\overline{OE}$) are common to all latches.

When pin LE is HIGH, data at the Dn inputs enters the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding Dn input changes. When pin LE is LOW, the latches store the information that is present at the Dn inputs, after a set-up time preceding the HIGH-to-LOW transition of LE.

When pin $\overline{OE}$ is LOW, the contents of the 8 latches are available at the outputs. When pin $\overline{OE}$ is HIGH, the outputs go to the high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

The 74AHC573; 74AHCT573 is functionally identical to:

- 74AHC563; 74AHCT563 which has inverted outputs and a different pin arrangement
- 74AHC373; 74AHCT373 which has a different pin arrangement

2. Features

- Balanced propagation delays
- All inputs have a Schmitt-trigger action
- Common 3-state output enable input
- Functionally identical to the 74AHC563; 74AHCT563 and 74AHC373; 74AHCT373
- Inputs accept voltages higher than V_{CC}
- Input levels:
  - For 74AHC573: CMOS input level
  - For 74AHCT573: TTL input level
- ESD protection:
  - HBM EIA/JESD22-A114E exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
  - CDM EIA/JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC573				
74AHC573D	–40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74AHC573PW	–40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74AHCT573				
74AHCT573D	–40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74AHCT573PW	–40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

4. Functional diagram

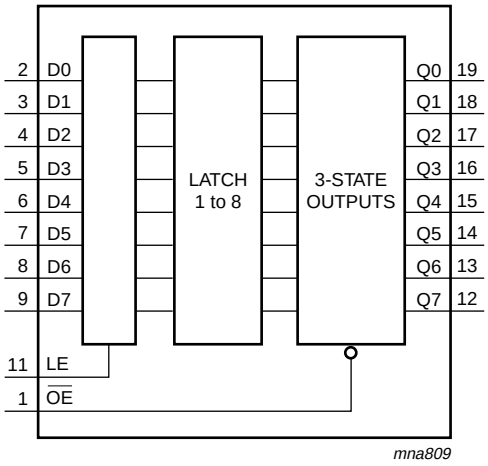


Fig 1. Functional diagram

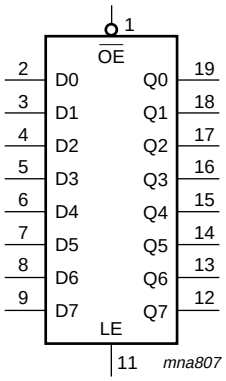


Fig 2. Logic symbol

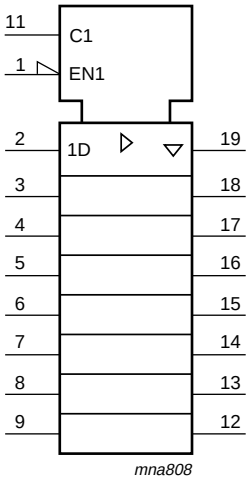


Fig 3. IEC logic symbol

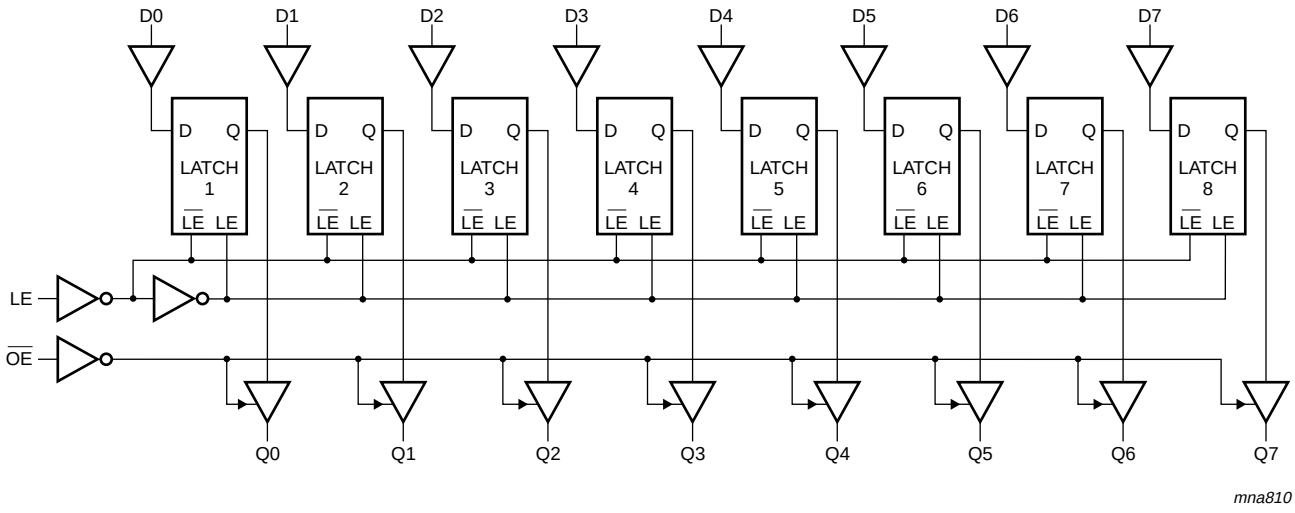


Fig 4. Logic diagram

5. Pinning information

5.1 Pinning

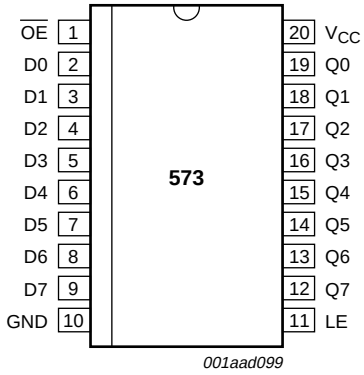


Fig 5. Pin configuration SO20 and TSSOP20

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{OE}$	1	3-state output enable input (active LOW)
D0	2	data input 0
D1	3	data input 1
D2	4	data input 2
D3	5	data input 3
D4	6	data input 4
D5	7	data input 5
D6	8	data input 6
D7	9	data input 7
GND	10	ground (0 V)
LE	11	latch enable input (active HIGH)
Q7	12	3-state latch output 7
Q6	13	3-state latch output 6
Q5	14	3-state latch output 5
Q4	15	3-state latch output 4
Q3	16	3-state latch output 3
Q2	17	3-state latch output 2
Q1	18	3-state latch output 1
Q0	19	3-state latch output 0
V_{CC}	20	supply voltage

6. Functional description

Table 3. Function table[1]

Operating mode	Input			Internal latch	Output
	$\overline{OE}$	LE	Dn		Q0 to Q7
Enable and read register (transparent mode)	L	H	L	L	L
			H	H	H
Latch and read register	L	L	l	L	L
			h	H	H
Latch register and disable outputs	H	L	l	L	Z
			h	H	Z

[1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition;
Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
V_I	input voltage			–0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V	[1]	–20	-	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	–20	+20	mA
I_O	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5$ V)		–25	+25	mA
I_{CC}	supply current			-	+75	mA
I_{GND}	ground current			–75	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO20 packages: above 70 °C the value of P_{tot} derates linearly at 8 mW/K.
For TSSOP20 packages: above 60 °C the value of P_{tot} derates linearly at 5.5 mW/K.

8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74AHC573						
V_{CC}	supply voltage		2.0	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 3.0 V to 3.6 V	-	-	100	ns/V
		V_{CC} = 4.5 V to 5.5 V	-	-	20	ns/V
74AHCT573						
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 4.5 V to 5.5 V	-	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C			Unit
			Min	Typ	Max	Min	Max	Min	Typ	Max	
74AHC573											
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	-	V
		V_{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	-	V
		V_{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	-	0.5	-	-	0.5	V
		V_{CC} = 3.0 V	-	-	0.9	-	0.9	-	-	0.9	V
		V_{CC} = 5.5 V	-	-	1.65	-	1.65	-	-	1.65	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}									
		I_O = –50 µA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	-	V
		I_O = –50 µA; V_{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	-	V
		I_O = –50 µA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	-	V
		I_O = –4.0 mA; V_{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	-	V
		I_O = –8.0 mA; V_{CC} = 4.5 V	3.94	-	-	3.80	-	3.70	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}									
		I_O = 50 µA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	-	0.1	V
		I_O = 50 µA; V_{CC} = 3.0 V	-	0	0.1	-	0.1	-	-	0.1	V
		I_O = 50 µA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.36	-	0.44	-	-	0.55	V
		I_O = 8.0 mA; V_{CC} = 4.5 V	-	-	0.36	-	0.44	-	-	0.55	V

Table 6. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C			Unit
			Min	Typ	Max	Min	Max	Min	Typ	Max	
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±0.25	-	±2.5	-	-	±10.0	µA
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	-	2.0	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	4.0	-	40	-	-	80	µA
C_I	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	-	10	pF
C_O	output capacitance		-	4	-	-	-	-	-	10	pF
74AHCT573											
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V									
		I_O = –50 µA	4.4	4.5	-	4.4	-	4.4	-	-	V
		I_O = –8.0 mA	3.94	-	-	3.80	-	3.70	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V									
		I_O = 50 µA	-	0	0.1	-	0.1	-	-	0.1	V
		I_O = 8.0 mA	-	-	0.36	-	0.44	-	-	0.55	V
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; I_O = 0 A	-	-	±0.25	-	±2.5	-	-	±10.0	µA
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	-	2.0	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	4.0	-	40	-	-	80	µA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC}$ – 2.1 V; I_O = 0 A; other pins at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V	-	-	1.35	-	1.5	-	-	1.5	mA
C_I	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	-	10	pF
C_O	output capacitance		-	4	-	-	-	-	-	10	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 10.

Symbol	Parameter	Conditions		25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	Min	Max	
74AHC573											
t_{pd}	propagation delay	Dn to Qn; see Figure 6	[2]								
		V_{CC} = 3.0 V to 3.6 V									
		C_L = 15 pF		-	5.5	11.0	1.0	13.0	1.0	14.0	ns
		C_L = 50 pF		-	7.8	14.5	1.0	16.5	1.0	18.5	ns
		V_{CC} = 4.5 V to 5.5 V									
		C_L = 15 pF		-	3.9	6.8	1.0	8.0	1.0	8.5	ns
		C_L = 50 pF		-	5.5	8.8	1.0	10.0	1.0	11.0	ns
		LE to Qn; see Figure 7	[2]								
		V_{CC} = 3.0 V to 3.6 V									
		C_L = 15 pF		-	5.8	11.9	1.0	14.0	1.0	15.0	ns
		C_L = 50 pF		-	8.3	15.4	1.0	17.5	1.0	19.5	ns
		V_{CC} = 4.5 V to 5.5 V									
		C_L = 15 pF		-	4.2	7.7	1.0	9.0	1.0	10.0	ns
		C_L = 50 pF		-	5.9	9.7	1.0	11.0	1.0	12.5	ns
t_{en}	enable time	$\overline{OE}$ to Qn; see Figure 8	[3]								
		V_{CC} = 3.0 V to 3.6 V									
		C_L = 15 pF		-	5.8	11.5	1.0	13.5	1.0	14.5	ns
		C_L = 50 pF		-	8.3	15.0	1.0	17.0	1.0	19.0	ns
		V_{CC} = 4.5 V to 5.5 V									
		C_L = 15 pF		-	4.4	7.7	1.0	9.0	1.0	10.0	ns
		C_L = 50 pF		-	6.3	9.7	1.0	11.0	1.0	12.5	ns
t_{dis}	disable time	$\overline{OE}$ to Qn; see Figure 8	[4]								
		V_{CC} = 3.0 V to 3.6 V									
		C_L = 15 pF		-	6.8	11.0	1.0	13.0	1.0	14.0	ns
		C_L = 50 pF		-	9.7	14.5	1.0	16.5	1.0	18.5	ns
		V_{CC} = 4.5 V to 5.5 V									
		C_L = 15 pF		-	4.6	7.7	1.0	9.0	1.0	10.0	ns
		C_L = 50 pF		-	7.4	9.7	1.0	11.0	1.0	12.5	ns
t_W	pulse width	LE HIGH; see Figure 7									
		V_{CC} = 3.0 V to 3.6 V		5.0	-	-	5.0	-	5.0	-	ns
		V_{CC} = 4.5 V to 5.5 V		5.0	-	-	5.0	-	5.0	-	ns
t_{su}	set-up time	Dn to LE; see Figure 9									
		V_{CC} = 3.0 V to 3.6 V		3.5	-	-	3.5	-	3.5	-	ns
		V_{CC} = 4.5 V to 5.5 V		3.5	-	-	3.5	-	3.5	-	ns

Table 7. Dynamic characteristics *…continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 10.

Symbol	Parameter	Conditions		25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	Min	Max	
t_h	hold time	Dn to LE; see Figure 9									
		V_{CC} = 3.0 V to 3.6 V		1.5	-	-	1.5	-	1.5	-	ns
		V_{CC} = 4.5 V to 5.5 V		1.5	-	-	1.5	-	1.5	-	ns
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC}	[5]	-	12	-	-	-	-	-	pF
74AHCT573; V_{CC} = 4.5 V to 5.5 V											
t_{pd}	propagation delay	Dn to Qn; see Figure 6	[2]								
		C_L = 15 pF		-	3.5	5.5	1	6.5	1	7.0	ns
		C_L = 50 pF		-	4.9	7.5	1	8.5	1	9.5	ns
		LE to Qn; see Figure 7	[2]								
		C_L = 15 pF		-	3.9	6.0	1	7.0	1	7.5	ns
		C_L = 50 pF		-	5.5	8.5	1	9.5	1	11.0	ns
t_{en}	enable time	$\overline{OE}$ to Qn; see Figure 8	[3]								
		C_L = 15 pF		-	4.1	6.5	1	7.5	1	8.5	ns
		C_L = 50 pF		-	5.9	8.5	1	10.0	1	11.0	ns
t_{dis}	disable time	$\overline{OE}$ to Qn; see Figure 8	[4]								
		C_L = 15 pF		-	4.5	6.5	1	7.5	1	8.5	ns
		C_L = 50 pF		-	6.4	9.0	1	10.0	1	11.5	ns
t_W	pulse width	LE HIGH; see Figure 7		5.0	-	-	5.0	-	5.0	-	ns
t_{su}	set-up time	Dn to LE; see Figure 9		3.5	-	-	3.5	-	3.5	-	ns
t_h	hold time	Dn to LE; see Figure 9		1.5	-	-	1.5	-	1.5	-	ns
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC}	[5]	-	18	-	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).

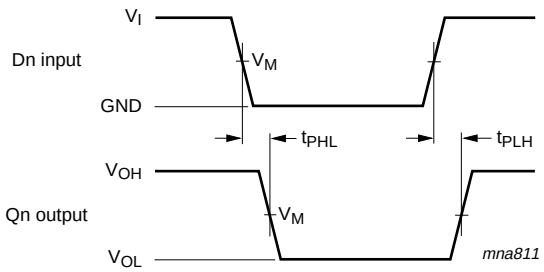
[2] t_{pd} is the same as t_{PHL} and t_{PLH}.

[3] t_{en} is the same as t_{PZH} and t_{PZL}.

[4] t_{dis} is the same as t_{PHZ} and t_{PLZ}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

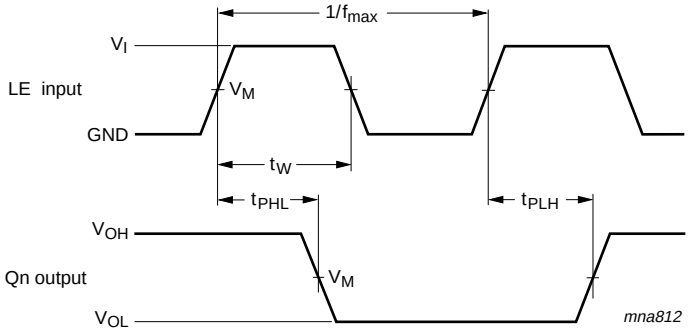
11. Waveforms



Measurement points are given in Table 8.

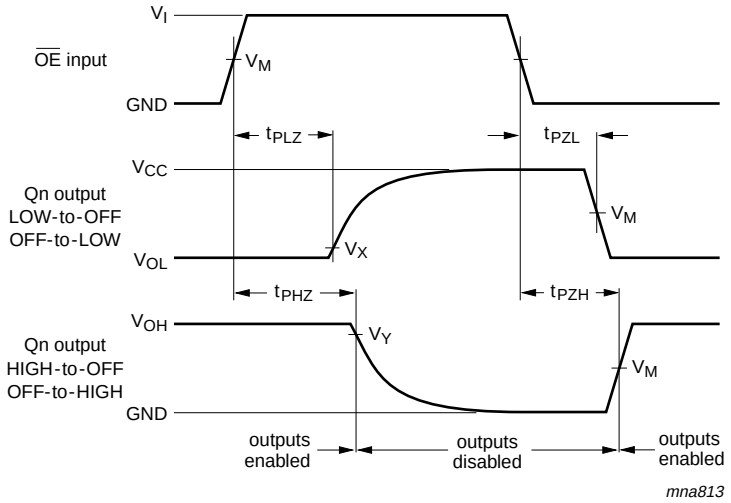
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Data input to output propagation delays



V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

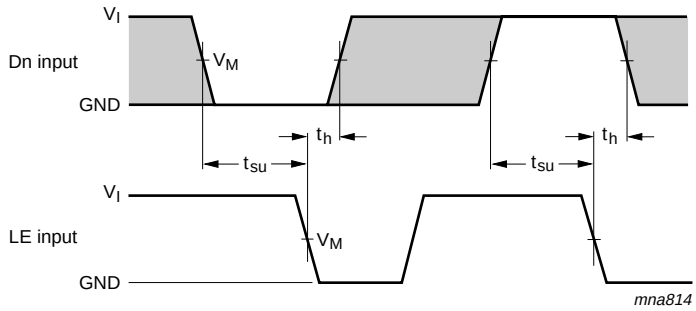
Fig 7. Latch enable input to output propagation delays



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 8. Enable and disable times



Measurement points are given in Table 8.

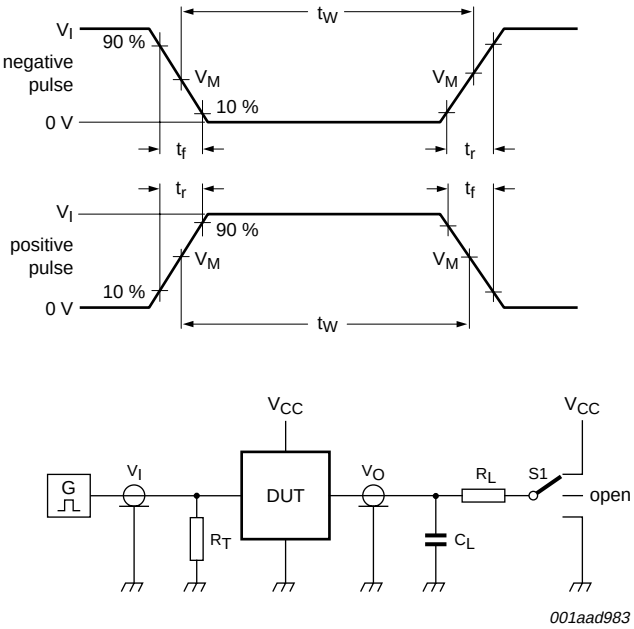
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

The shaded areas indicate when the input is permitted to change for predicable output performance.

Fig 9. Data set-up and hold times

Table 8. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74AHC573	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{OL} + 0.3 V	V_{OH} − 0.3 V
74AHCT573	1.5 V	$0.5 \times V_{CC}$	V_{OL} + 0.3 V	V_{OH} − 0.3 V



Test data is given in Table 9.

Definitions test circuit:

R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

R_L = load resistance.

S1 = test selection switch.

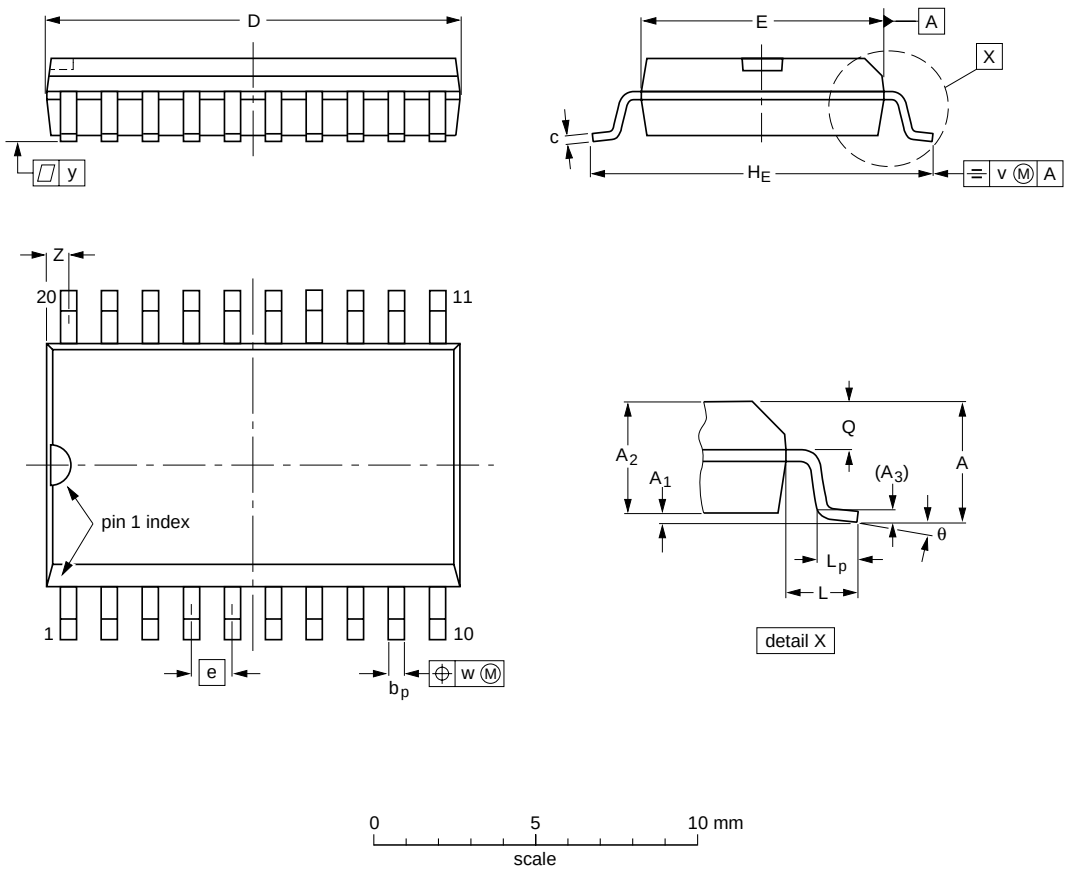
Fig 10. Test circuitry for switching times

Table 9. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74AHC573	V_{CC}	≤ 3.0 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}
74AHCT573	3.0 V	≤ 3.0 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}

12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

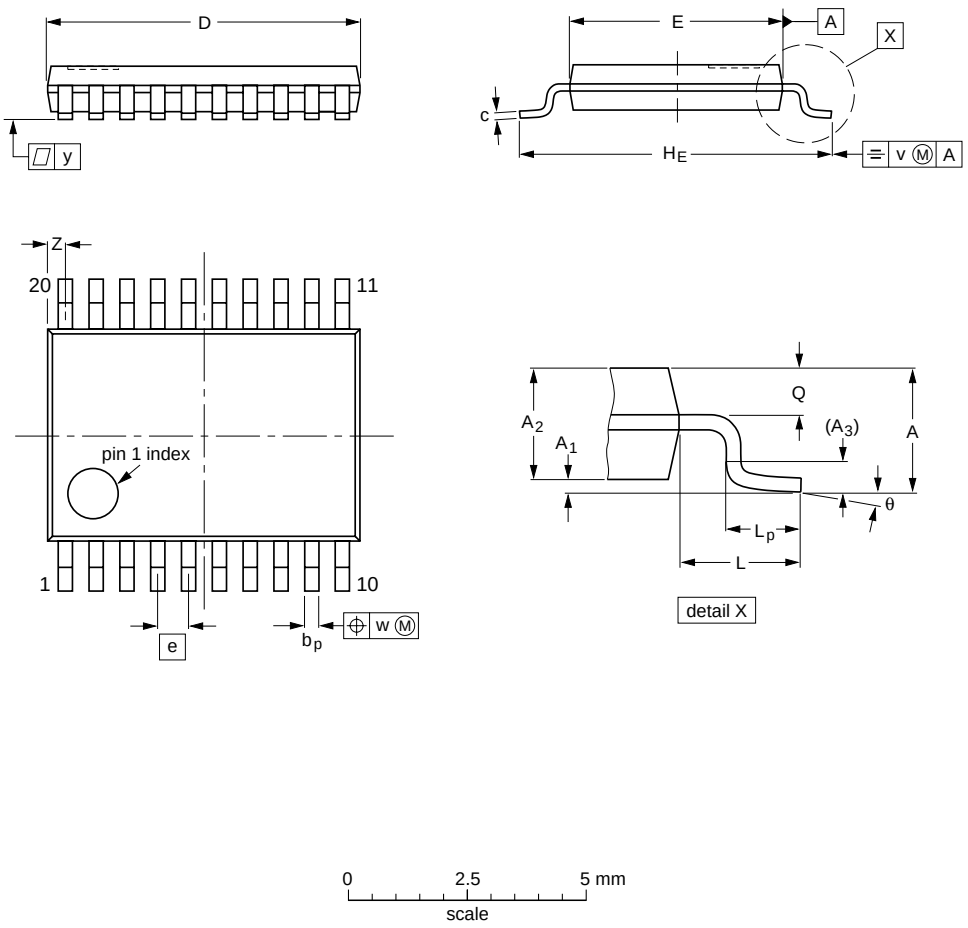
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig 12. Package outline SOT360-1 (TSSOP20)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT573_3	20080424	Product data sheet	-	74AHC_AHCT573_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 6: conditions for the input leakage current have been changed.			
74AHC_AHCT573_2	20031208	Product specification	-	74AHC_AHCT573_1
74AHC_AHCT573_1	19990927	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

15.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

17. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 24 April 2008

Document identifier: 74AHC_AHCT573_3